**Mid-Term Sample Practice Questions**

1. The most appropriate matching for the following pairs is-

**Column-1:**

X: Indirect addressing

Y: Immediate addressing

Z: Auto decrement addressing

**Column-2:**

1. Loops

2. Pointers

3. Constants

1. X-3, Y-2, Z-1
2. X-1, Y-3, Z-2
3. X-2, Y-3, Z-1
4. X-3, Y-1, Z-2

Ans: (c)

1. In the absolute/direct addressing mode:
2. The operand is inside the instruction
3. The address of the operand is inside the instruction
4. The register containing the address of the operand is specified inside the instruction
5. The location of the operand is implicit

Ans: (b)

1. Which of the following addressing modes are suitable for program relocation at run time?
2. Absolute addressing
3. Base addressing
4. Relative addressing
5. Indirect addressing

1. 1 and 4
2. 1 and 2
3. 2 and 3
4. 1, 2 and 4

Ans: (c)

1. What is the most appropriate match for the items in the first column with the items in the second column?

**Column-1:**

X: Indirect addressing

Y: Indexed addressing

Z: Base register addressing

**Column-2:**

1. Array implementation

2. Writing relocatable code

3. Passing array as parameter

1. X-3, Y-1, Z-2
2. X-2, Y-3, Z-1
3. X-3, Y-2, Z-1
4. X-1, Y-3, Z-2

Ans: (a)

1. Which of the following addressing modes permits relocation without any change whatsoever in the code?
2. Indirect addressing
3. Indexed addressing
4. Base register addressing
5. PC relative addressing

Ans: (d)

1. Consider the following memory values and a one-address machine with an accumulator, what values do the following instructions load into accumulator?

* Word 20 contains 40
* Word 30 contains 50
* Word 40 contains 60
* Word 50 contains 70

Instructions are-

1. Load immediate 20
2. Load direct 20
3. Load indirect 20
4. Load immediate 30
5. Load direct 30
6. Load indirect 30

 Ans: (a) 20 (b) 40 (c) 60 (d) 30 (e) 50 (f) 70

7. The addressing mode/s, which uses the PC instead of a general-purpose register is\_\_\_\_\_\_

a) Indexed with offset

b) Relative

c) Direct

d) Both Indexed with offset and direct

Ans: (b)

1. The addressing mode which makes use of in-direction pointers is \_\_\_\_\_\_  
   a) Indirect addressing mode  
   b) Index addressing mode  
   c) Relative addressing mode  
   d) Offset addressing mode

Ans: (a)  
Explanation: In this addressing mode, the value of the register serves as another memory location and hence we use pointers to get the data.

1. In the following indexed addressing mode instruction, MOV 5(R1), LOC the effective address is \_\_\_\_\_\_  
   a) EA = 5+R1  
   b) EA = R1  
   c) EA = [R1]  
   d) EA = 5+[R1]

Ans: (d)

10. When we use auto increment or auto decrements, which of the following is/are true?  
1. In both, the address is used to retrieve the operand and then the address gets altered  
2. In auto increment, the operand is retrieved first and then the address altered  
3. Both of them can be used on general purpose registers as well as memory locations  
a) 1, 2, 3  
b) 2  
c) 1, 3  
d) 2, 3

Ans: (d)

Explanation: In the case of, auto increment the increment is done afterward and in auto decrement the decrement is done first.

11. The addressing mode, where you directly specify the operand value is \_\_\_\_\_\_\_  
a) Immediate  
b) Direct  
c) Definite  
d) Relative

Ans: (a)

12.  \_\_\_\_\_ addressing mode is most suitable to change the normal sequence of execution of instructions.  
a) Relative  
b) Indirect  
c) Index with Offset  
d) Immediate

Ans: a

Explanation: The relative addressing mode is used for this since it directly updates the PC.

13. How many bits of opcode is required to implement a CPU with 10 arithmetic and logical instructions, 2 control instructions, and 5 data transfer instructions?

1. 2
2. 3
3. 4
4. 5

Ans: (d)

14. Which of the following options represents the correct matching?

Table

Description automatically generated

1. 1->A; 2->D; 3->C; 4->B;
2. 1->C; 2->B; 3->D; 4->A;
3. 1->C; 2->B; 3->A; 4->D;
4. 1->A; 2->D; 3->B; 4->C;

Ans: (c)

15. An instruction is stored at location 500 with its address field at location 501. The address field has the value 600. A processor register R1 contains the number 300. The effective address will be if the addressing mode is: (i) Immediate (ii) Absolute (iii) Indirect (iv) Relative (v) Index with R1 as index register (vi) Base Register Addressing Mode (vii) Base Index Register AM (viii) Register Indirect AM

16. Calculate the address line and data lines in the following memory:

(i) 4K x 1 (ii) 16K x 16 (iii) 32GB (iv) 16M x 16 (v) 8KB

17. How many 8K x 8 memory chips are required to design 16MB memory?

18. Calculate the effective address for the following register:

1) SS: 3860H, SP: 1735H, BP: 4826H

2) The value of the DS register is 3032H. And the BX register contains a 16-bit value which is equal to 3032H. 0008H is added to BX.  
 ADD BX, 0008H  
The register AX contains some value which needs to be stored at a location as follows:  
 MOV [BX], AX  
Calculate the address at which the value of the AX will be stored.

19. Define and explain the concept of pipelining used in 8086 MPU.

20. What do you mean by the term interrupt? Give the difference between the following interrupts:

(i) Vectored and Non-Vectored Interrupts

(ii) Maskable and Non-maskable Interrupts.

21. Perform the following and tell the status of each flag used in 8086:

(i) 110001 + 111011

(ii) 1FFF H - 2000 H

22. In 2’s compliment representation, if two numbers with the same sign are added, then

(i) Overflows occur if and only if the results have opposite sign.

(ii) Overflows occur if and only if the results have same sign.

(iii) Both (a) and (b)

(iv) Overflows does not occur

23. Using Booth’s Algorithm for multiplication, the multiplier -57 will be recoded as  
(A) 0 -1 0 0 1 0 0 -1  
(B) 1 1 0 0 0 1 1 1  
(C) 0 -1 0 0 1 0 0 0  
(D) 0 1 0 0 -1 0 0 1

24. Consider that the memory is byte addressable with size 32 bits, and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs while the CPU has been halted after executing the HALT instruction, the return address (in decimal) saved in the stack will be

25. Which of the following is/are true of the auto-increment addressing mode?

I. It is useful in creating self-relocating code.

II. If it is included in an Instruction Set Architecture, then an additional ALU is required for effective address calculation.

III. The amount of increment depends on the size of the data item accessed.

1. I only  
   (B) II only  
   (C) III Only  
   (D) II and III only

26. Consider a memory system, in which the cache access time is 100ns and the memory access time is 1200 ns. If we would like to have average access time to be or more than 20% higher than cache access time, then the hit ratio of the cache must at least be

a) 85% b) 82% c) 98% d) 99%

27. In two level hierarchy, the top level has an access time of 10ns, and bottom level has an access time of 50ns, the hit rate on the top level is 90%. If the block size of cache is 16 bytes, then what is the average memory access time required? (Consider the system uses locality of reference)

28. In two level hierarchy, the cache has an access time of 12ns and the main memory access time of 120ns, the hit rate of cache is 90%. If the block size of cache is 16 bytes, then what is the average memory access time including Miss Penalty? (Miss Penalty: Time to bring main memory block to cache memory when cache miss occurs)

29. The BIU contains FIFO register of size bytes

A. 8 B. 6 C. 4 D. 12

ANSWER: B

30. The BIU prefetches the instruction from memory and store them in

A. queue B. register C. memory D. stack

ANSWER: A

31. The 1 MB byte of memory can be divided into segment

A. 1 Kbyte B. 64 Kbyte C. 33 Kbyte D. 34 Kbyte

32. Define and explain the concept of pipelining.

33. Explain the function of Instruction Queue Residing in 8086 MPU.

34. Draw and Explain the architecture of 8086 MPU.

35. Define and draw the flag register of 8086 MPU. Explain the function of each flag in detail.

36 Define the following terms used in 8086 MPU: (i) Instruction Pointer (ii) Stack Pointer (iii) Pipelining (iv)

37. Instruction Pointer (IP) contains offset address of \_\_\_\_\_\_\_\_ segment.

a) Data segment

b) Code segment

c) Stack segment

d) Extra segment

Answer: b

38. If the memory access takes 20 ns with cache and 110 ns without it, then the hit ratio, (cache uses a 10 ns memory) is,

a) 93% b) 87% c) 88% d) 90%

Ans: d)

39. If the cache needs an access time of 20 ns and the main memory 120ns, then the average access time of a CPU is (assuming hit ration is 80%)

a) 40ns b) 35ns c) 30ns d) 45ns

Ans: a)

40. For a memory system, hit time is given as 2 ns with miss rate of 1.5% and miss penalty of 60 ns then average access time is

a) 2.98 ns b) 2.9 ns c) 4.19 ns d) 3.98 ns

Ans: b)

41. For a memory system, the average access time is 4.5 ns with hit time 3 ns and miss rate of 2.5% then miss penalty is

a)80 ns b) 100 ns c) 60 ns d) 55 ns

Ans: c)

42. The memory read operation takes 20 ns as cache access time, and 28 ns as main memory access time, h = 6/7 then what will be the mean access time

a)16ns b) 48ns c) 28ns d) 24ns

Ans: d)

43. For a machine assume that the cache miss penalty is 50 clock cycles, and all instruction normally takes 2 clock cycles. Assume that the miss rate is 2% and there is an average of 1.33 memory references per instruction. What is impact on performance when behaviour of cache is included?

a)68.5 b) 58.7 c) 78.2 d) None of these

Ans: a)

43. In a two-level cache memory hierarchy, the access time of L1 cache, L2 cache, and main memory access cache is 15 ns, 30 ns, and 1000 ns, respectively. The hit rates of L1 and L2 caches are 0.6 and 0.7, respectively. What is the average access time of the system?

1) Including the cache time within the search.

2) Ignoring the cache time within the search.

44. Define the following terms used in cache memory:

1) Cache hit

2) Cache hit time

3) Cache Miss

4) Miss Time Penalty

5) Hit Ratio

6) Cache Mapping

7) Locality of Reference

8) Spatial Reference

9) Temporal Reference.

45. Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find-

1) Number of bits in tag

2) Tag directory size

3) Physical address bit

46. Consider a direct mapped cache of size 512 KB with block size 1 KB. There are 7 bits in the tag. Find-

1) Size of main memory

2) Tag directory size

47. Use the Booth algorithm to multiply -54 (multiplicand) by 19 (multiplier), where each number is represented using 6 bits. Show the procedure in detail.

48. Use the Booth algorithm to multiply 54 (multiplicand) by -19 (multiplier), where each number is represented using 6 bits. Show the procedure in detail.

49. Use the Booth algorithm to multiply 54 (multiplicand) by 19 (multiplier), where each number is represented using 6 bits. Show the procedure in detail.

50. Use the Booth algorithm to multiply -54 (multiplicand) by -19 (multiplier), where each number is represented using 6 bits. Show the procedure in detail.